3.3V CMOS 32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCH32373A

FEATURES:

- **Typical tSK(o) (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **VCC = 3.3V ± 0.3V, Normal Range**
- **VCC = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **All inputs, outputs, and I/O are 5V tolerant**
- **Supports hot insertion**
- **Available in 96-ball LFBGA package**

DRIVE FEATURES:

- **Balanced Output Drivers: ±24mA**
- **Reduced system switching noise**

APPLICATIONS:

- **5V and 3.3V mixed voltage systems**
- **Data communication and telecommunication systems**

DESCRIPTION:

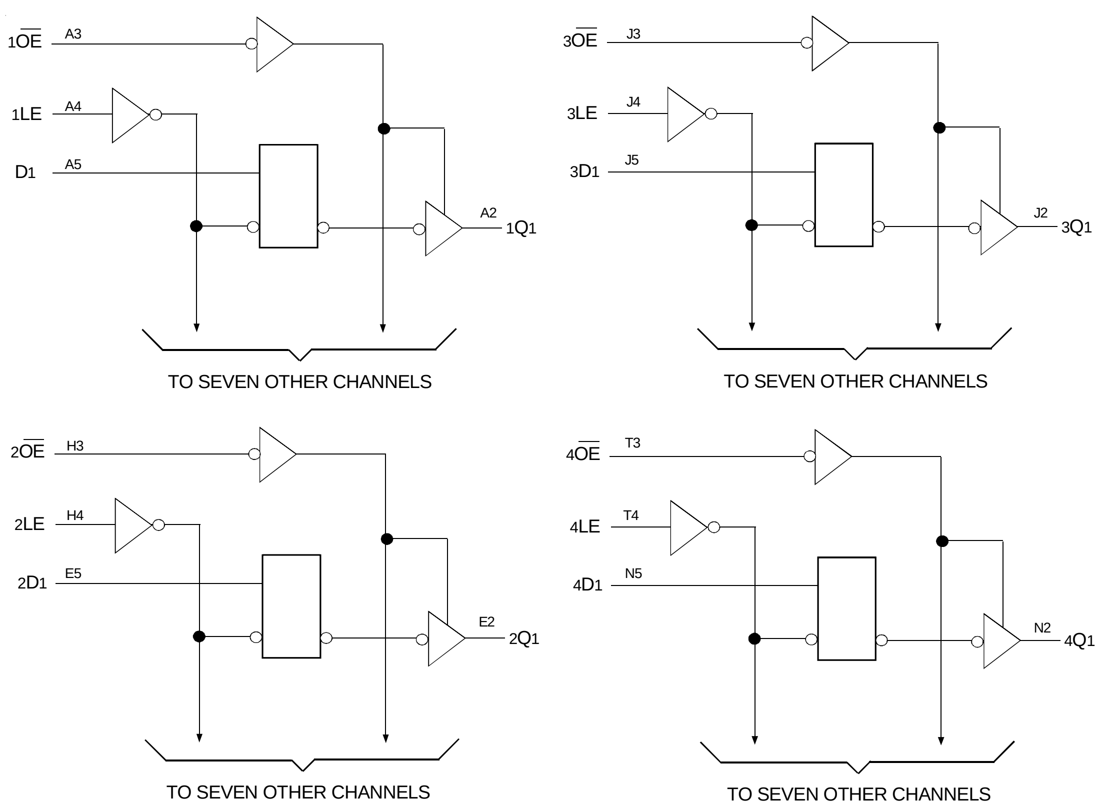
The LVCH32373A 32-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. The device can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as four 8-bit latches, two 16-bit latches, or one 32-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of the LVCH32373A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH32373A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH32373A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

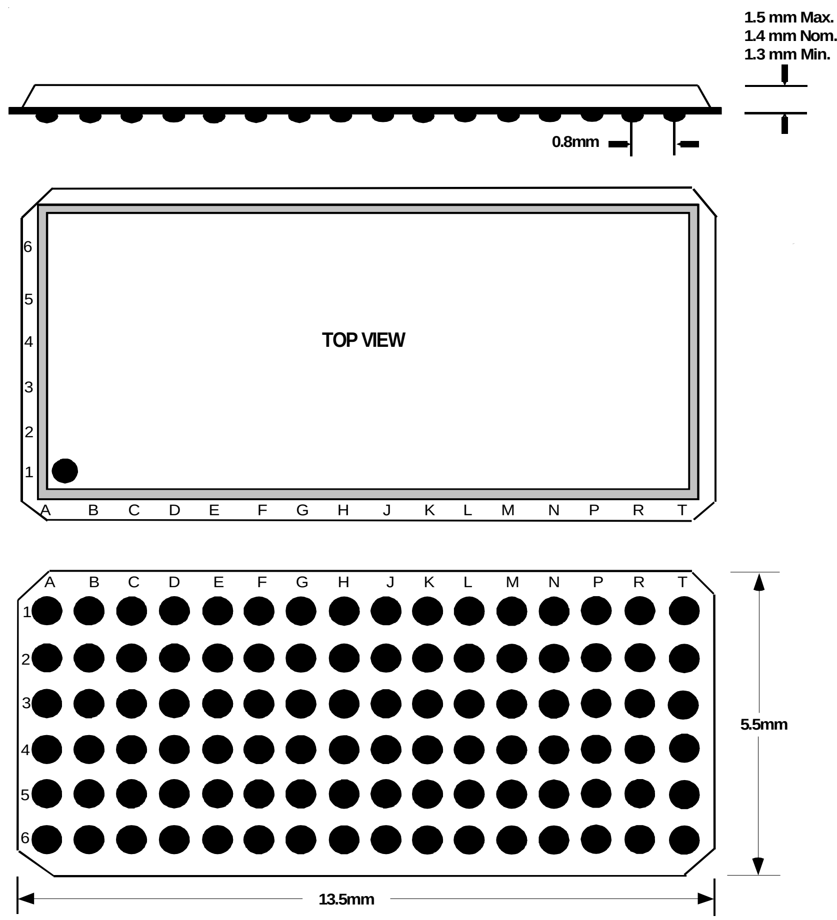


PIN CONFIGURATION

6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1LE	GND	VCC	GND	GND	VCC	GND	2LE	3LE	GND	VCC	GND	GND	VCC	GND	4LE
3	1$\overline{OE}$	GND	VCC	GND	GND	VCC	GND	2$\overline{OE}$	3$\overline{OE}$	GND	VCC	GND	GND	VCC	GND	4$\overline{OE}$
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

LFBGA
TOPVIEW

96 BALL LFBGA PACKAGE ATTRIBUTES



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +6.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, V_I < 0 or V_O < 0	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs(1)
xLE	Latch Enable Inputs (Active HIGH)
x$\overline{OE}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH 8-BIT SECTION)(1)

Inputs			Outputs
x$\overline{OE}$	xLE	xDx	xQx
L	H	H	H
L	H	L	L
H	X	X	Z
L	L	X	Q(2)

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level of Q before the indicated steady-state conditions were established.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3V	V_I = 2V	–75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	—	—	—	µA
I_{BHL}			V_I = 0.7V	—	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	±500	µA

NOTES:
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
			$3.6 \leq V_{IN} \leq 5.5V$(2)	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	500	µA

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per Latch Outputs enabled	C_L = 0pF, f = 10Mhz	78	pF
C_{PD}	Power Dissipation Capacitance per Latch Outputs disabled		12	

SWITCHING CHARACTERISTICS(1)

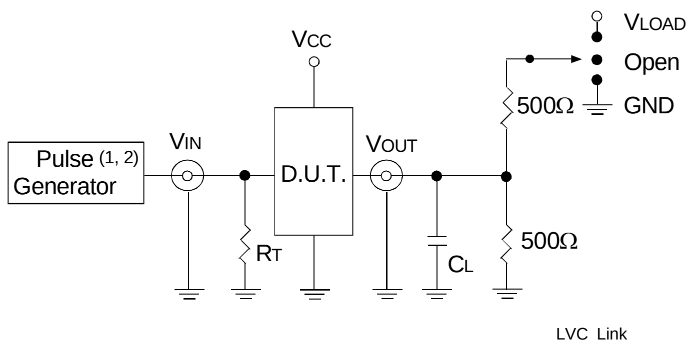
Symbol	Parameter	V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xDx to xQx	1.5	4.9	1.6	4.2	ns
t_{PLH} t_{PHL}	Propagation Delay xLE to xQx	2	5.3	2.1	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	1.5	5.7	1.3	4.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	1.5	6.3	2.5	5.9	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xLE	1.7	—	1.7	—	ns
t_H	Hold Time HIGH or LOW, xDx after xLE	1.2	—	1.2	—	ns
t_W	xLE Pulse Width HIGH	3.3	—	3.3	—	ns
$t_{SK(o)}$	Output Skew(2)	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	Vcc(1)=3.3V±0.3V	Vcc(1)=2.7V	Vcc(2)=2.5V±0.2V	Unit
VLOAD	6	6	2 x Vcc	V
VIH	2.7	2.7	Vcc	V
VT	1.5	1.5	Vcc / 2	V
VLZ	300	300	150	mV
VHZ	300	300	150	mV
CL	50	50	30	pF



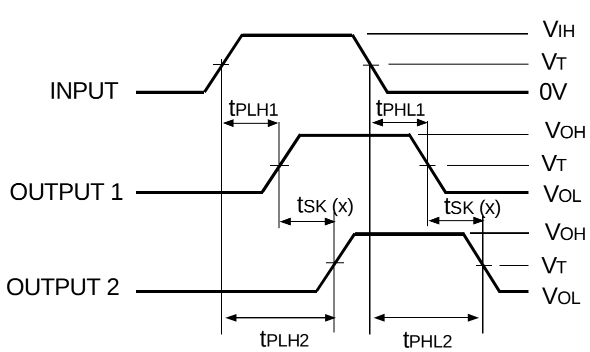
Test Circuit for All Outputs

DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2ns; tR ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	VLOAD
Disable High Enable High	GND
All Other Tests	Open

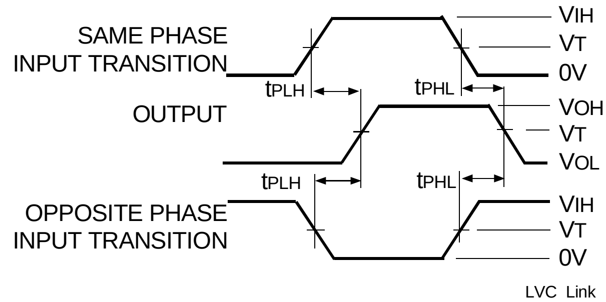


tSK(x) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

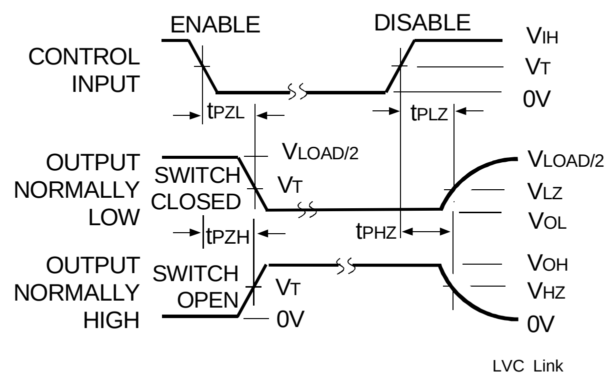
Output Skew - tSK(x)

LVC Link

NOTES:
1. For tSK(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tSK(b) OUTPUT1 and OUTPUT2 are in the same bank.

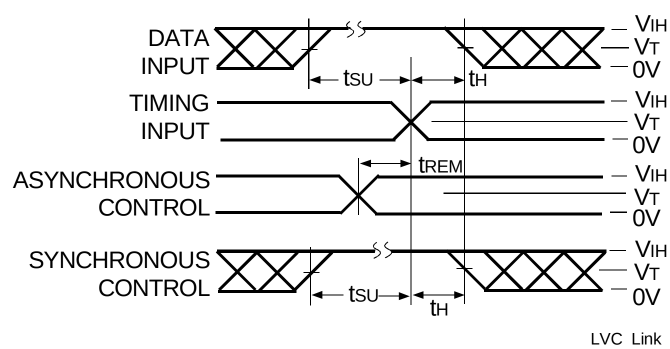


Propagation Delay

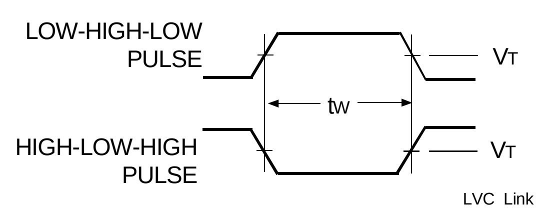


Enable and Disable Times

NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT XX LVC X XX XXXX XX

Field	Code	Description
Package	BF	Low-Profile Fine Pitch Ball Grid Array
Device Type	373A	32-Bit Transparent D-Type Latch with 5V Tolerant I/O
Family	32	32-bit Bus Density, ±24mA
Bus-Hold	H	Bus-hold
Temp. Range	74	-40°C to +85°C

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